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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/809,181	03/16/2001	Toshiya Satoh	503.39864X00	5733

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EXAMINER

DIAZ, JOSE R

ART UNIT PAPER NUMBER

2815

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 09/809,181	Applicant(s) SATO ET AL	
	Examiner José R Díaz	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 19 December 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-10 and 28-36 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 28-36 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-4, 28-29, 33 and 35-36 rejected under 35 U.S.C. 102(e) as being anticipated by Nagai et al. (US 2002/0130412 A1).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1 and 33, Nagai et al. teaches a semiconductor device comprising: semiconductor elements (1) (see fig. 4) obtained by cutting a semiconductor wafer having an integrated circuit (see paragraph [0029]) and an electrode pad (2) (see fig. 4) formed on one side along a cutting scribe line (consider the boundaries, i.e. each end side, of the substrate 1, as shown in fig. 4), a stress cushioning layer (3) installed on said semiconductor elements (1) (see fig. 4), a lead

Art Unit: 2815

wire portion (4) extending from said electrode pad (2) to a top of said stress cushioning layer (3) through an opening (consider the portions of the substrate 1 not covered by the stress cushioning layer 3) formed in said stress cushioning layer on said electrode pad (see fig. 4), external electrode (6) arranged on said lead wire portion on top of said stress cushioning layer (see fig. 4), and a conductor protective layer (5) installed on said stress cushioning layer excluding said external electrode arrange on said lead wire portion (see figs. 2f and 4), wherein said stress cushioning layer (3), said lead wire portion (4), said conductor protective layer (5), and said external electrodes (6) have means for forming each end face on an end surface of said semiconductor elements inside said cutting scribe line (please note that the stress cushioning layer 3, the lead wire portion 4, the conductor protective layer 5, and the external electrodes 6 do not extend beyond the side boundaries of the semiconductor elements 1, see fig. 2) and exposing a range (the area between the pad 2 and the end side of the substrate 1) from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line, such that said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes are located inside of a peripheral edge of said semiconductor elements (see fig. 2).

Regarding claim 3 and 35, Nagai et al. teaches that the conductor protective layer (5) is formed outside the end face of the stress-cushioning layer (3) (see fig. 4).

Regarding claims 4 and 36, Nagai et al. teaches that the end area (area adjacent to the pad 2) of said stress cushioning layer (3) is formed so as to become tapered and thinner toward the end face of the stress-cushioning layer (3) (see fig. 2).

Regarding claims 28-29, Nagai et al. teaches that the stress-cushioning layer is comprised of a pasty polyimide material or a low elastomeric material (see paragraph [0038]).

Claims 1, 3-5, 7-8, 10, 28-31, 33 and 35-36 rejected under 35 U.S.C. 102(e) as being anticipated by Shimoishizaka et al. (US Pat. No. 6,313,532 B1).

Regarding claims 1 and 33, Shimoishizaka et al. teaches a semiconductor device comprising: semiconductor elements (10) (see fig. 7) obtained by cutting a semiconductor wafer having an integrated circuit (see col. 5, lines 62-66) and an electrode pad (11) (see figs. 8(a)-8(d)) formed on one side along a cutting scribe line (consider the boundaries, i.e. each end side, of the substrate 10, as shown in fig. 7), a stress cushioning layer (20) installed on said semiconductor elements (10) (see fig. 7), a lead wire portion (31) extending from said electrode pad (11) to a top of said stress cushioning layer (20) through an opening (consider the portion of the substrate 10 not covered by the stress cushioning layer 20) formed in said stress cushioning layer on said electrode pad (see figs. 7 and figs. 8(a)-8(d)), external electrode (40) arranged on said lead wire portion on top of said stress cushioning layer (see fig. 7), and a conductor protective layer (50) installed on said stress cushioning layer excluding said external electrode arrange on said lead wire portion (see fig. 7), wherein said stress cushioning layer (20), said lead wire portion (31), said conductor protective layer (50), and said external electrodes (40) have means for forming each end face on an end surface of said semiconductor elements inside said cutting scribe line (please note that the stress

cushioning layer 20, the lead wire portion 31, the conductor protective layer 50, and the external electrodes 40 do not extend beyond the boundaries of the semiconductor elements 10, see fig. 7), and exposing a range (the portion of the substrate 10 not covered by the stress cushioning layer 20) from said end face (consider the end side of the stress cushioning layer 20) on said end surface of said semiconductor elements (10) to an inside of said cutting scribe line (consider the boundary boundaries of the semiconductor elements 10, see fig. 7).

In addition and with regards to claim 5, Shimoishizaka et al. teaches a semiconductor element protective layer (12) installed on said semiconductor elements (10) (see fig. 7); the stress cushioning layer (20) installed on said semiconductor element protective layer (12) (see fig. 7), a first opening (consider the portion of the substrate 10 not covered by the protective layer 12) formed in said semiconductor element protective layer (12) on said electrode pad (11) (see figs. 8(a)-8(d)), a second opening (consider the portion of the substrate 10 not covered by the stress cushioning layer 20) in said stress cushioning layer (20) on said electrode pad (11) (see figs. 8(a)-8(d)), wherein said semiconductor element protective layer (12) has an end face on an end surface of said semiconductor elements inside said cutting scribe line (please note that the semiconductor element protective layer 12 does not extend beyond the boundaries of the semiconductor elements 10, see figs. 7 and 8(a)-8(d)).

Regarding claims 3, 7 and 35, Shimoishizaka et al. teaches that end face of the conductor protective layer (50) is formed outside the end face of the stress-cushioning layer (20) (see fig. 7).

Regarding claims 4, 10 and 36, Shimoishizaka et al. teaches that the end area of said stress cushioning layer (20) is formed so as to become tapered and thinner toward the end face of the stress-cushioning layer (20) (see figs. 7 and 8(a)-8(d)).

Regarding claim 8, Shimoishizaka et al. teaches that the end face of the semiconductor element protective layer (12) is formed outside the end face of the stress-cushioning layer (20) (see figs. 7 and 8(a)-8(d)).

Regarding claims 28-31, Shimoishizaka et al. teaches that the stress-cushioning layer is comprised of a pasty polyimide material or a low elastomeric material (see col. 7, lines 42-45).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 3, 5, 7, 9, 28-33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (US Pat. No. 6,452,270 B1) in view of Yamamoto (JP 10-092685).

Regarding claims 1, 5 and 33, Huang teaches a semiconductor device comprising: semiconductor elements (310) (see fig. 8) obtained by cutting a semiconductor wafer having an integrated circuit (400) (see fig. 8) and an electrode pad (320) (see fig. 8) formed on one side along a cutting scribe line (consider the boundaries, i.e. end side, of the substrate 310, as shown in fig. 8), a passivation layer (320) installed on said semiconductor elements (310) (see fig. 8), a lead wire portion (440) extending from said electrode pad (320) to a top of said passivation layer (320) through an opening (consider the portion not covered by the passivation layer 320) formed in said passivation layer (320) on said electrode pad (see fig. 8), external electrode (470) arranged on said lead wire portion on top of said passivation layer (320) (see fig. 8), and a conductor protective layer (450) installed on said passivation layer (320), excluding said external electrode arrange on said lead wire portion (see fig. 8), wherein said passivation layer (320), said lead wire portion (440), said conductor protective layer (450), and said external electrodes (470) have means for forming each end face on an end surface of said semiconductor elements inside said cutting scribe line (please note that said passivation layer 320, the lead wire portion 440, the conductor protective layer 450, and the external electrodes 470 do not extend beyond



Art Unit: 2815

the boundaries of the semiconductor elements 310, see fig. 8), and exposing a range (consider the portion of the substrate 310 not covered by the passivation layer 330 and the pad 320) from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line (consider the end sides of the substrate 310) (see fig. 8).

However, Huang fails to teach the limitation about the stress cushioning layer and/or the semiconductor element protective layer.

Yamamoto teaches that it is very well known in the art to include a multi-layered stress-cushioning structure comprised of a semiconductor element protective layer (17) and the stress-cushioning layer (15), and formed between the passivation layer (16) and lead wire portion (14) (see fig. 2 and abstract). Further, Yamamoto teaches first and second openings (consider portions of the pad 13 not covered by the semiconductor element protective layer and the stress-cushioning layer) formed in said semiconductor element protective layer (17) layer and the stress-cushioning layer (15) to exposed the pad (13).

Huang and Yamamoto are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a semiconductor element protective layer and a stress-cushioning layer installed between the semiconductor elements and lead wire portion so that the semiconductor element protective layer, the stress cushioning layer, the lead wire portion, the conductor protective layer, and the external electrodes have means for forming each end face on an end surface of the

Art Unit: 2815

semiconductor elements inside the cutting scribe line . The motivation for doing so, as is taught by Yamamoto, is to provide a wiring structure with high reliability and reducing manufacturing cost (paragraphs [0007] and [0010]). Therefore, it would have been obvious to combine Yamamoto with Huang to obtain the invention of claims 1, 3, 5, 7, 9, 28-33 and 35.

Regarding claims 3, 7 and 35, Huang teaches that the end face of the conductor protective layer (450) is formed outside the end face of the passivation layer (330) (see fig. 8), and Yamamoto further teaches the formation of the stress-cushioning layer (15) on said passivation layer (16) (see fig. 2).

Regarding claim 9, Yamamoto teaches that the semiconductor protective layer (17) is formed inside the end face of the stress-cushioning layer (15) (please note that the semiconductor element protective layer 17 does not extend beyond the end face of the stress-cushioning layer located near the boundaries of the substrate 12, see fig. 2).

Regarding claims 28-31, Yamamoto teaches that the stress-cushioning layer is comprised of a pasty polyimide material or a low elastomeric material (see paragraph [0013] of translation).

Regarding claim 32, Yamamoto teaches that the semiconductor element protective layer (17) is made of, for example, polyimide (see last two sentences of paragraph [0013] of translation).

Art Unit: 2815

Claims 2, 6 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (US Pat. No. 6,452,270 B1) in view of Yamamoto (JP 10-092685), and further in view of Okada et al. (US Pat. No. 6,111,317).

Regarding claims 2, 6 and 34, a further difference between the prior art and the claimed invention is the limitation about an end face of the conductor protective layer formed inside the end face of the stress-cushioning layer. Okada et al. teaches that it is well known in the art to form conductor protective layer (15) so that the end sides of the conductor protective layer (15) do not extend beyond the end sides of the wiring portion (14, 16, and 24) (see fig. 17).

Okada et al., Huang and Yamamoto are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to further include an end face of the conductor protective layer formed inside the end face of the stress-cushioning layer. The motivation for further doing so, as is taught by Okada et al., is to provide a low cost manufacturing method and to prevent a connection failure between semiconductor devices (col. 9, lines 19-21). Therefore, it would have been obvious to further combine Okada et al. with Huang and Yamamoto to obtain the invention of claims 2, 6 and 34.

### ***Response to Arguments***

Applicant's arguments, see remarks, filed December 19, 2003, with respect to claims 1-10, and 28-36 have been fully considered and are persuasive. The previous rejections of claims 1-10 and 28-36 have been withdrawn.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references teach the formation of a bump electrode over a semiconductor substrate: Hosomi et al. (US Pat. No. 5,773,888), Matsuda et al. (US Pat. No. 5,757,078), Hashimoto (US Pat. No. 6,608,389 B1), and Inoue et al. (US Pat. No. 6,624,504 B1).

### ***Correspondence***

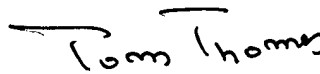
Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on 9:00-5:00 Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2815

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JRD  
3/17/04

  
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